Characterization of C^2MOS Flip-Flop in Sub-Threshold Region

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Outline

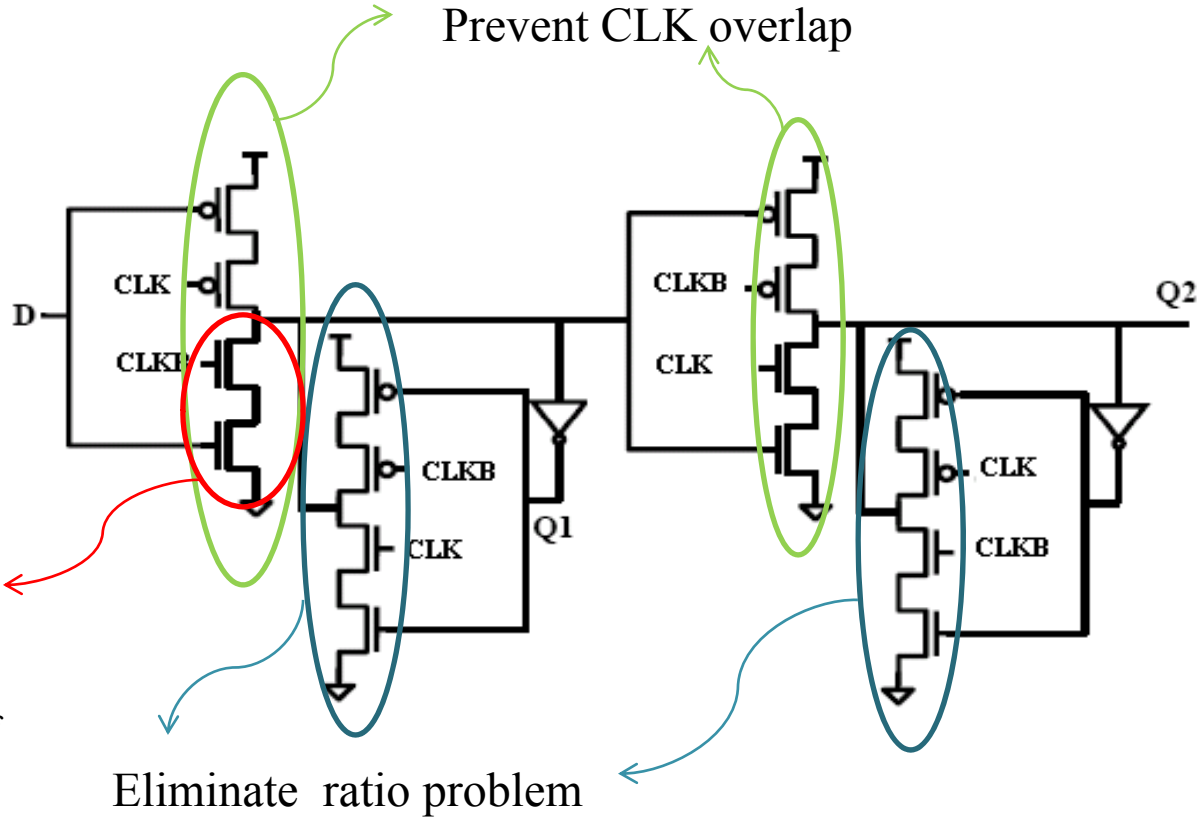
- Motivation
- Energy & Delay comparison of different types of Flip-Flops
- Timing characterization of C^2MOS
- Vdd & Size Effects
- Conclusion
- References

Motivation

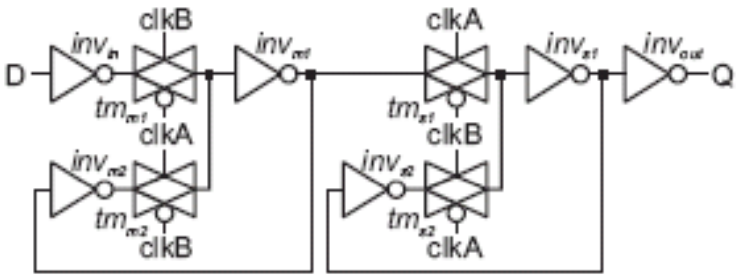
- Sub-threshold circuits are one of the solution to the ultra-low energy systems while Flip-Flops are essential timing blocks in digital circuits.
- t_{su}, t_{hold}, $t_{c\text{-}q}$ are affected by process variation.
- Timing & energy characterization of sub-threshold Flip-Flops should be performed for correct design of Flip-Flops.

Motivation

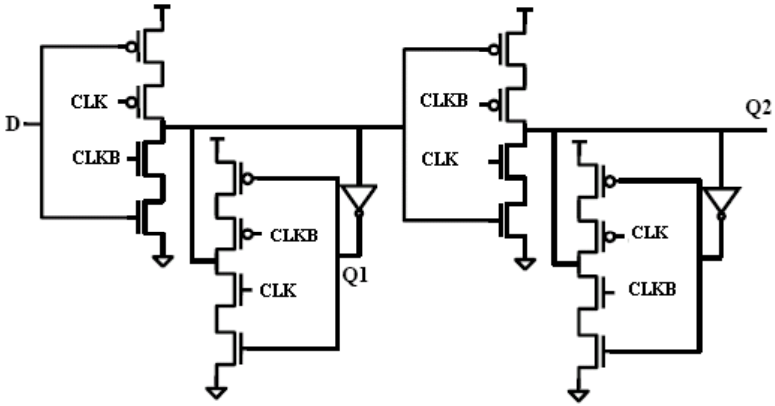
- C^2MOS FF is one of the promising Flip-Flops in sub-threshold circuits.



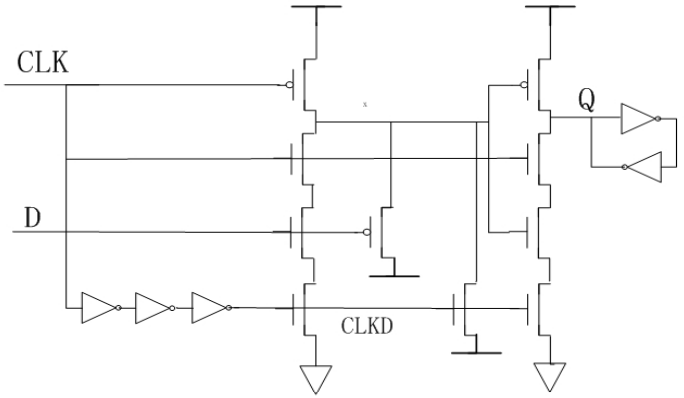
Energy & Delay Comparison of 4 types of FFs



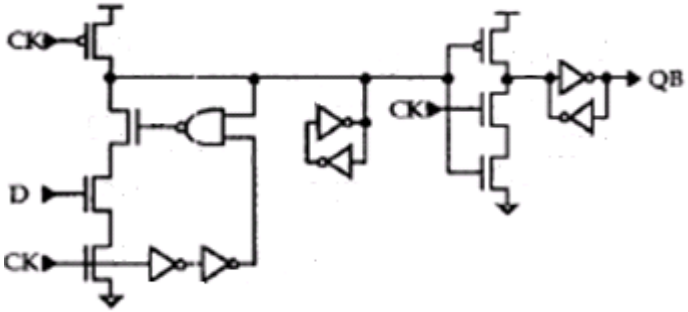
TGFF



C²MOS



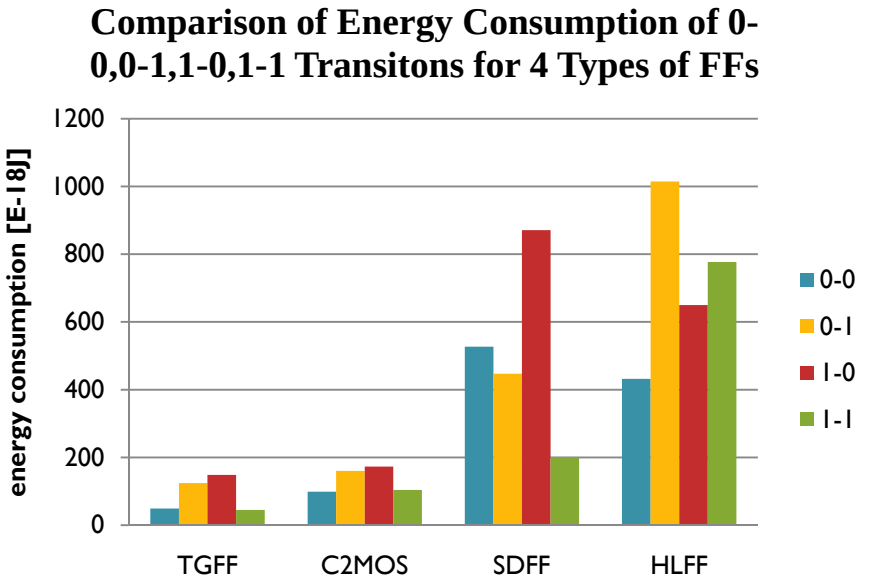
HLFF

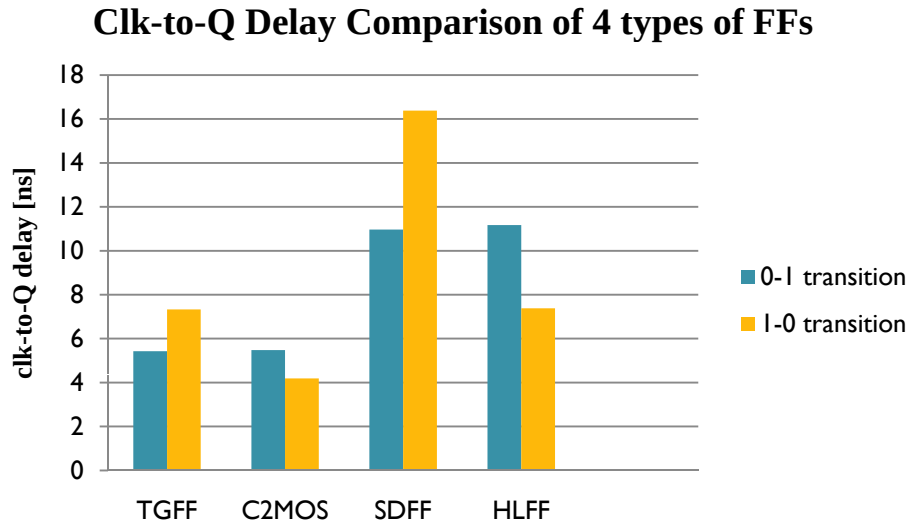


SDFF

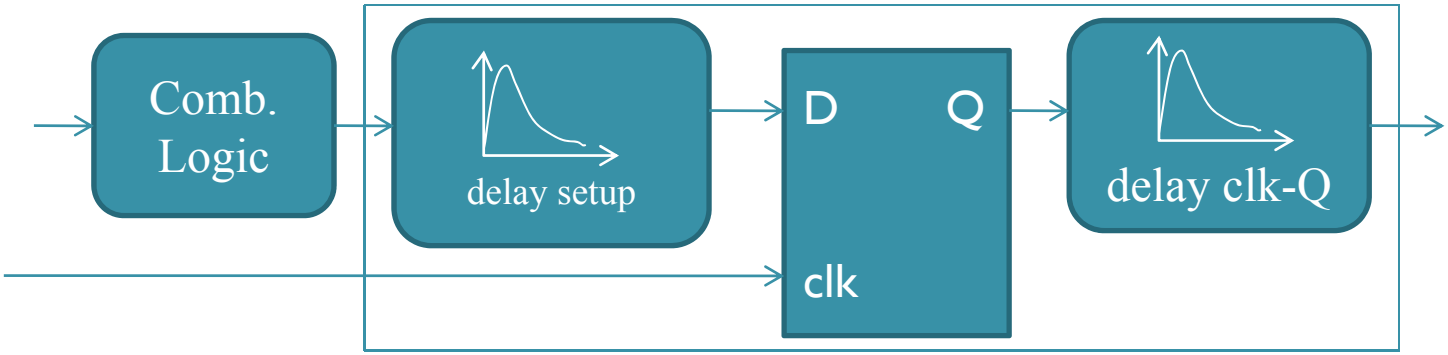
Comparison Results

- Low power consumption compared with SDFF and HLFF
- Power consumption is almost the same as TGFF but C²MOS can release the clock overlap problem while TGFF cannot.
- C²MOS has lower clk-to-Q delay.





Timing Characterization



- The setup time of the Flip-Flop has a lognormal pattern due to the output of the combinational logic.
- The setup time will result in the failure of functionality. It should be noted that the setup and hold time should be in the safe operation region to ensure the correct functionality.

Result

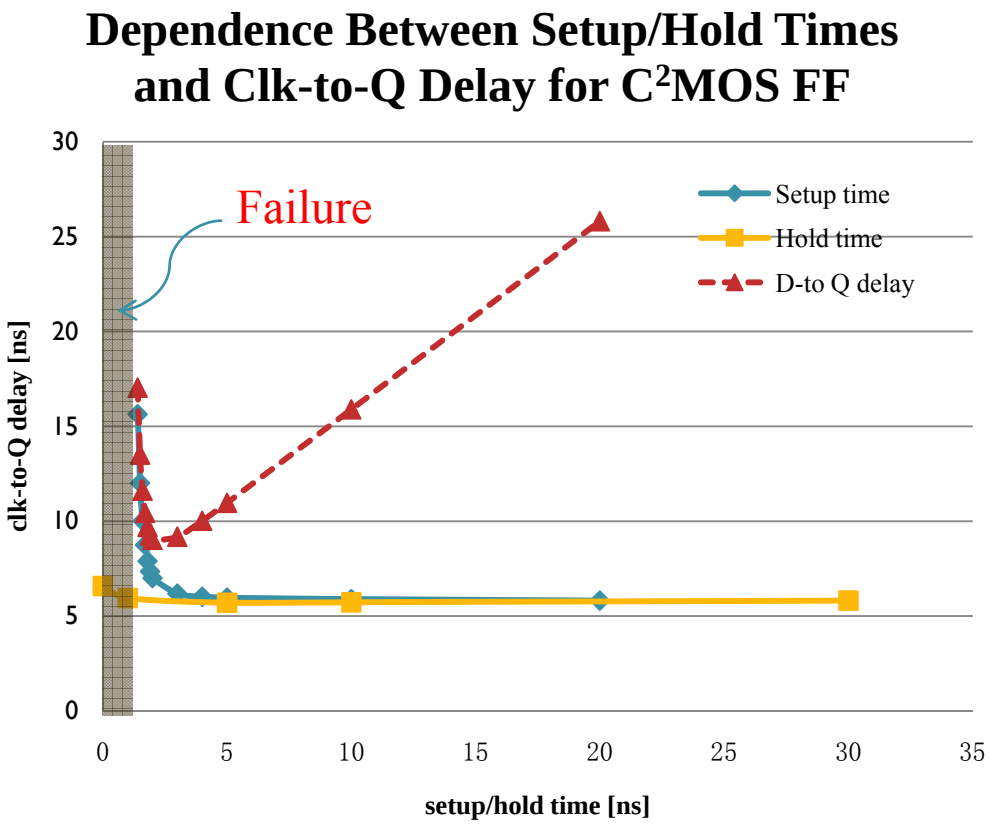
- Parameters Definition:

  t_{su}: time from D input valid to the triggering edge

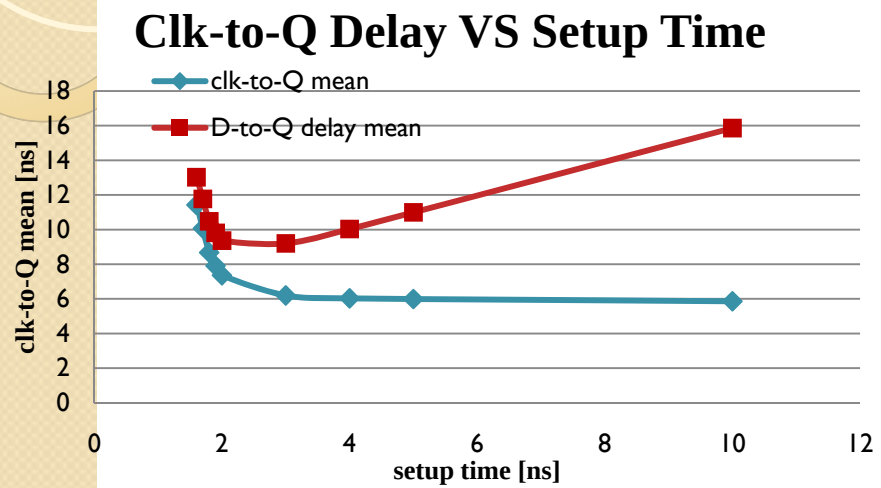
  t_{hold}: time for which the D input is valid after the triggering edge

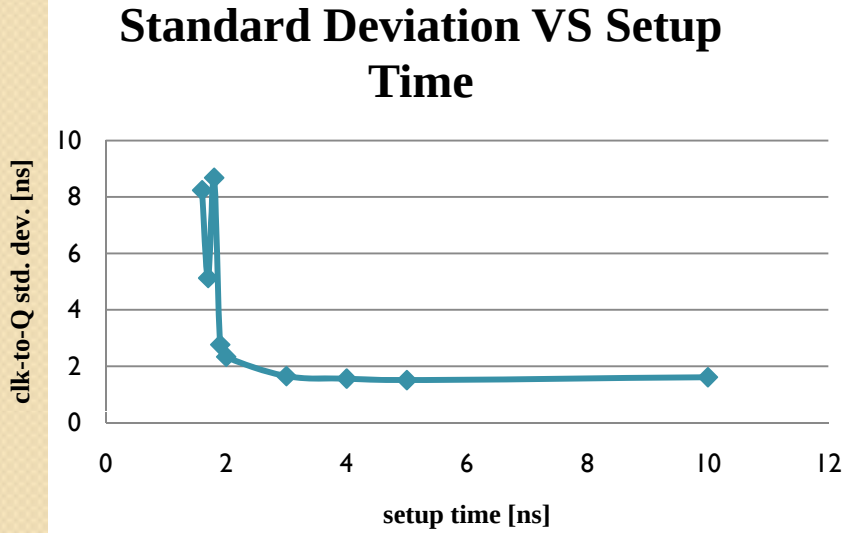
  clk-to-Q delay: time from the triggering edge until valid data is available at Q output

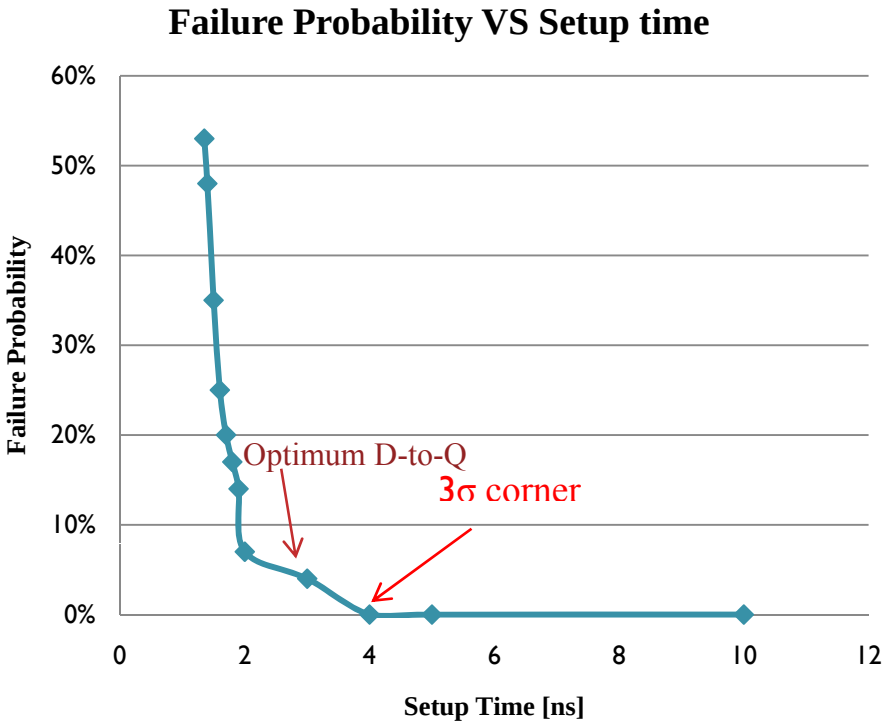
- Failure of the functionality due to the metastability of the Flip-Flops



Variability of Timing Using Monte-Carlo Simulation

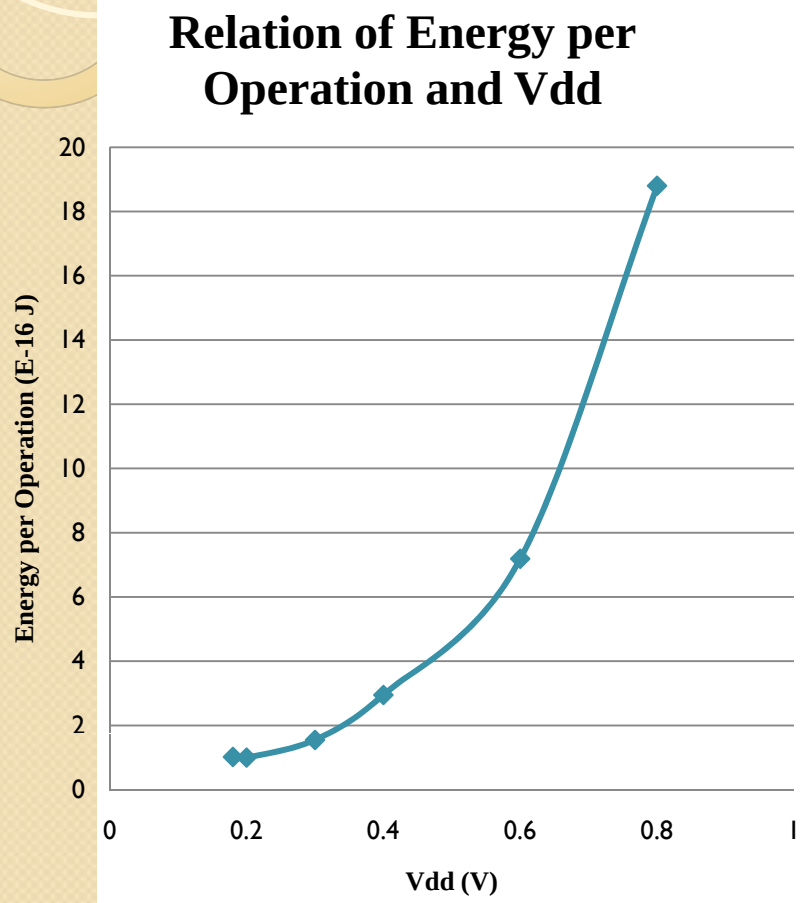


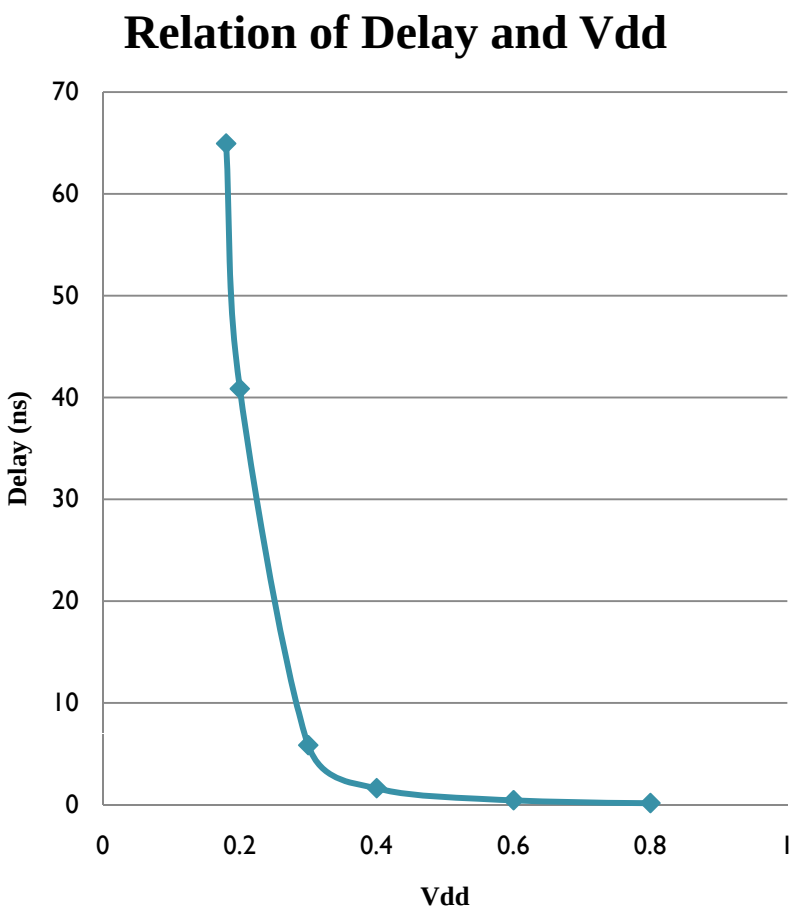




The FF becomes reliability-driven instead of optimum-timing driven in sub-threshold region.

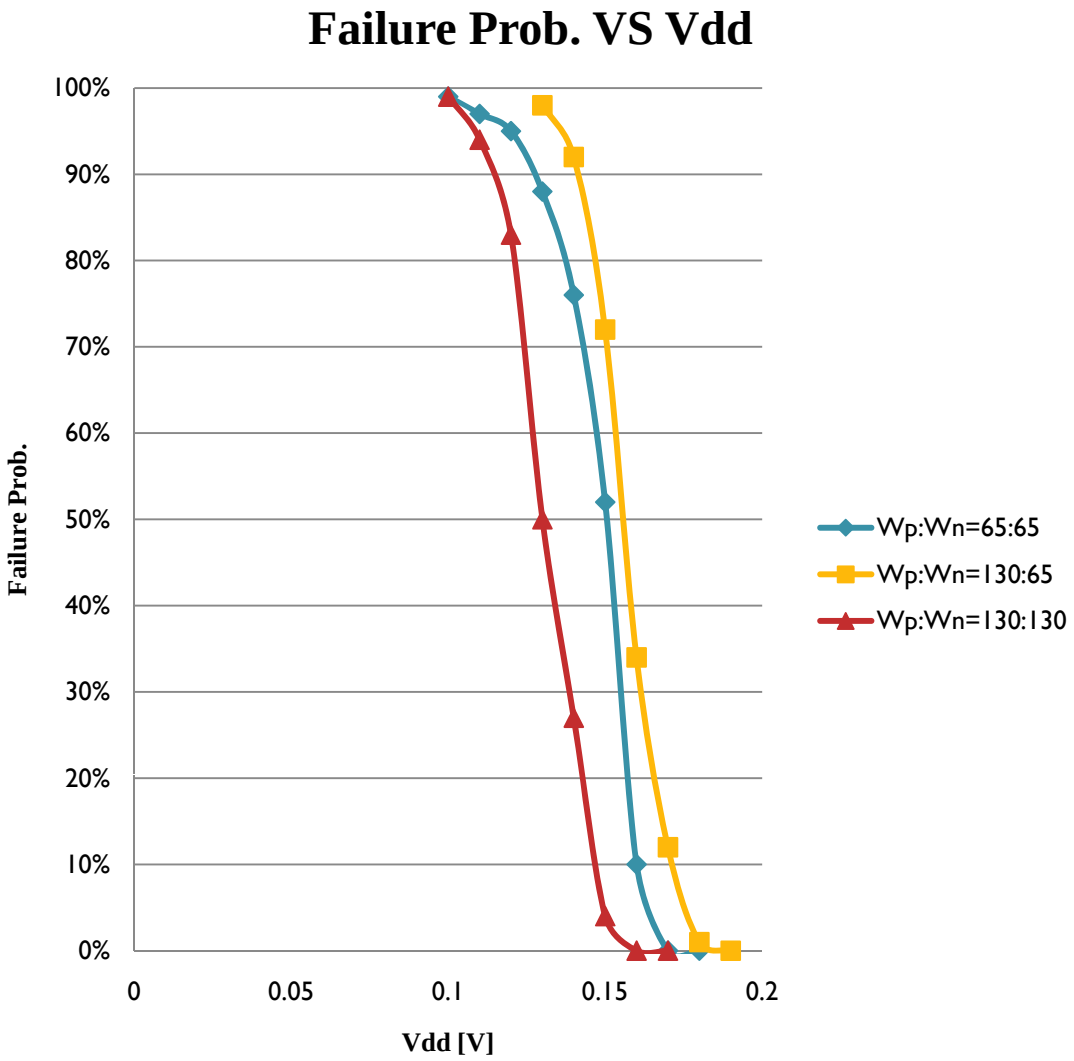
Turning Knobs - Vdd



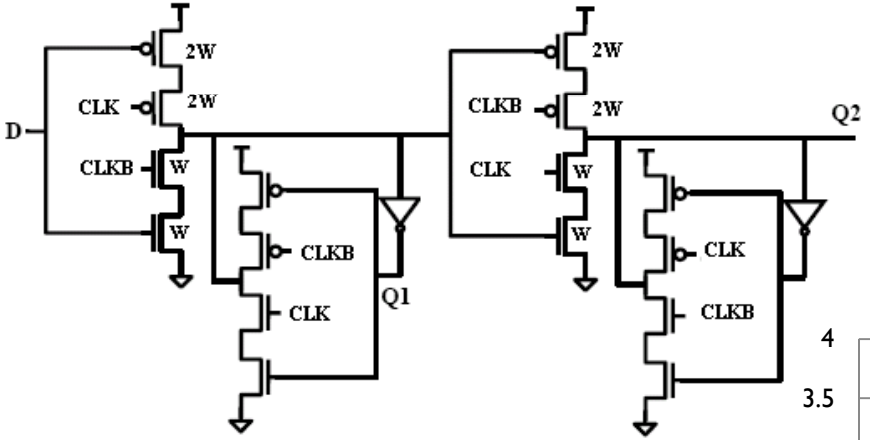


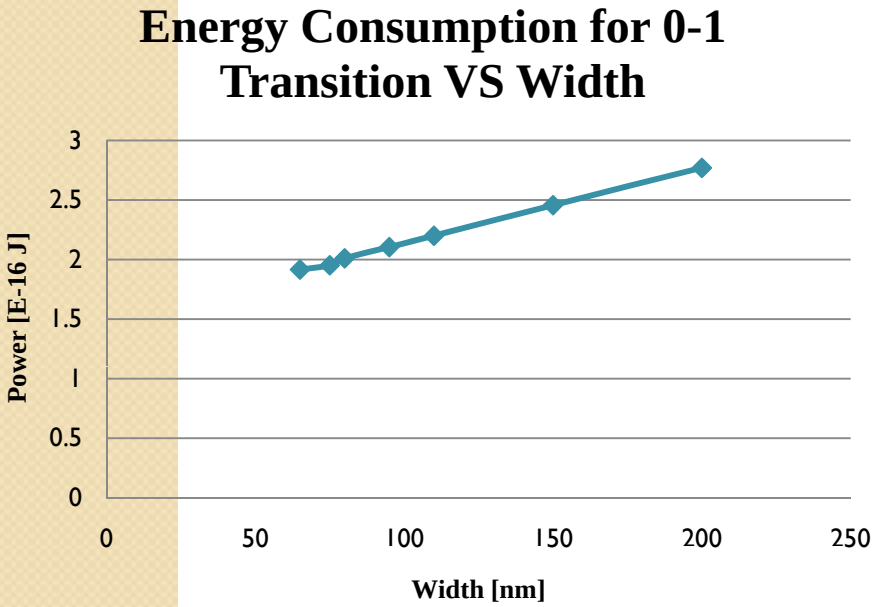
Failure Prob. VS Vdd for Different Sizes

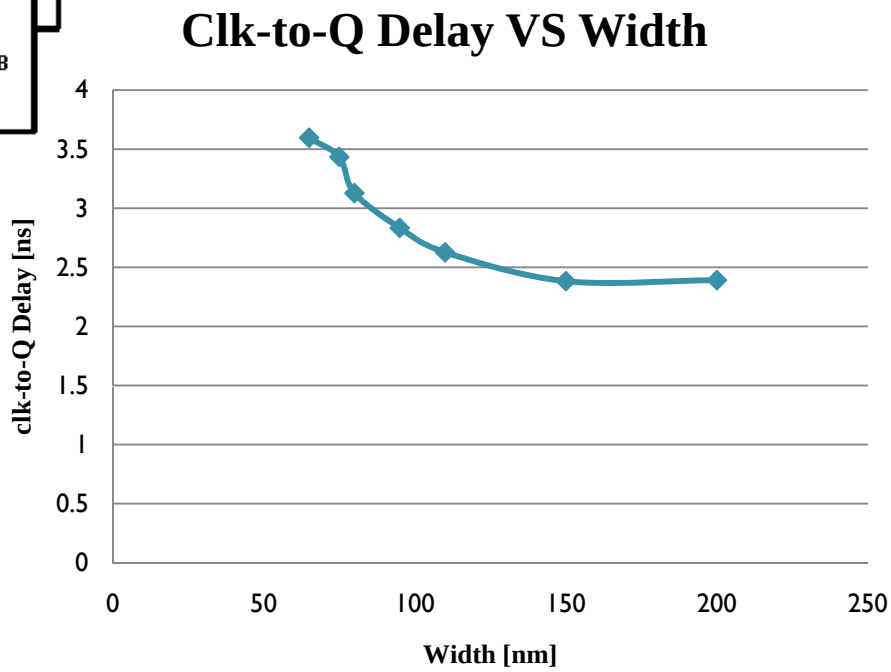
- 65:65 circuits has higher failure probability than 130:130 circuits due to larger effects of process variation on smaller size devices.
- Unbalanced PMOS and NMOS circuit shows higher failure probability possibly because of unbalanced effects of variation on weak and strong devices.



Turning Knobs - Size

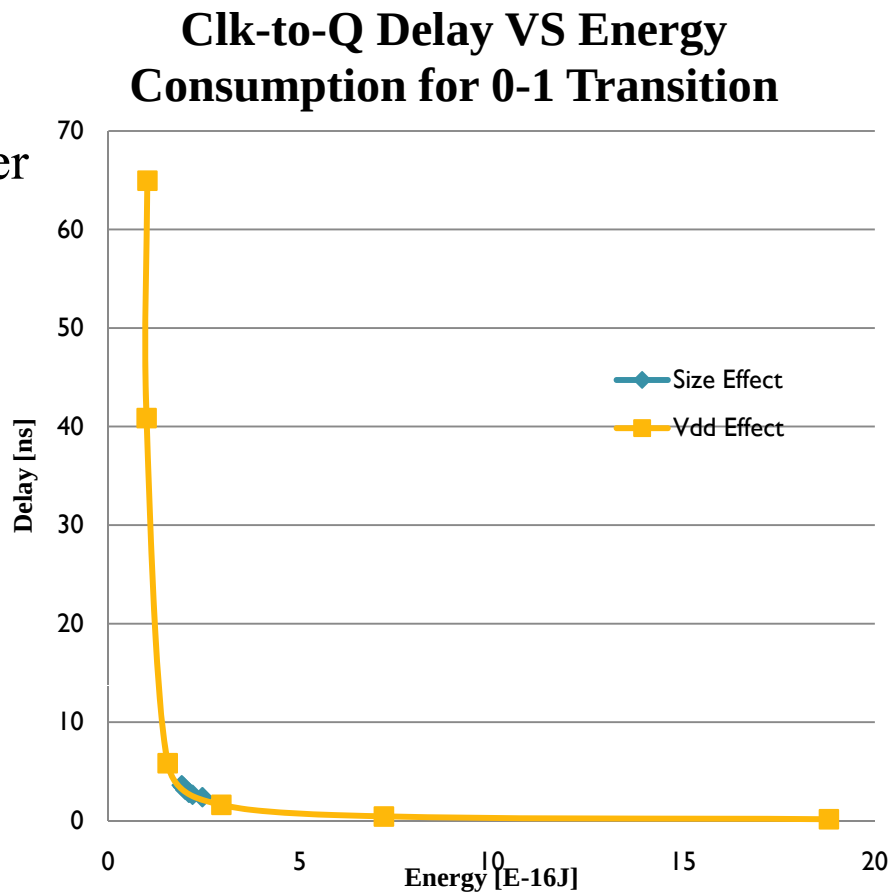






Energy – Delay Relationship

- Size has smaller effect compared with Vdd effect since the former has only linear effect while the latter has exponential effect.



Conclusion

- A timing model for FF operating at sub-threshold voltages has been used to characterize C^2MOS Flip-Flop.
- It has been shown that optimum-timing design should be replaced by reliability-driven design for subthreshold Flip-Flops.
- Size has effect on failure probability due to process variation.
- Size has minor effect on the performance while Vdd has large effect on performance due to its exponential character in current equation.

References

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